

## CLAIMS

What is claimed is:

- 1 1. A method of executing a sequence of instructions comprising:
  - 2 comparing a first plurality of least significant bits (LSBs) of a first operand
  - 3 to a second plurality of LSBs of a second operand to determine a
  - 4 predicted predicate value (PPV) for a predicate;
  - 5 and
  - 6 conditionally executing a predicated instruction depending on the PPV.
- 1 2. The method of claim 1, further comprising:
  - 2 executing a COMPARE instruction to determine an actual predicate value
  - 3 (APV) for the predicate;
  - 4 comparing the APV to the PPV; and
  - 5 flushing a pipeline if the APV and the PPV are unequal.
- 1 3. The method of claim 2, further comprising executing the predicated  
2 instruction after flushing the pipeline.
- 1 4. The method of claim 2, wherein flushing the pipeline comprises flushing only  
2 a backend portion of the pipeline.

1 5. The method of claim 2, further comprising updating historical information  
2 corresponding to the predicate in a predicate history table after comparing the  
3 APV to the PPV.

1 6. The method of claim 1, wherein comparing the first plurality to the second  
2 plurality includes comparing the least significant quarter or less of the first  
3 operand bits to the least significant quarter or less of the second operand  
4 bits.

1 7. The method of claim 1, wherein conditionally executing the predicated  
2 instruction includes executing the predicated instruction if the PPV is true.

1 8. The method of claim 7, wherein conditionally executing the predicated  
2 instruction includes treating the predicated instruction like a no-op if the PPV  
3 is false.

1 9. The method of claim 1, wherein comparing the first plurality to the second  
2 plurality is done after determining a low confidence level in an ability to  
3 accurately calculate the PPV based on historical information associated with  
4 the predicate.

1 10. A method of executing a sequence of instructions comprising:

2 determining a confidence level in an ability to accurately calculate a  
3 predicted predicate value (PPV) for a predicate based on historical  
4 information associated with the predicate;  
5 determining the PPV using the historical information if the confidence level  
6 is determined to be a first level; and  
7 determining the PPV by comparing a first plurality of least significant bits  
8 (LSBs) of a first operand of a COMPARE instruction to a second  
9 plurality of LSBs of a second operand of the COMPARE instruction if  
10 the confidence level is determined to be a second level.

1 11. The method of claim 10, further comprising:

2 conditionally executing a predicated instruction depending on the PPV;  
3 determining an actual predicate value (APV) for the predicate; and  
4 flushing a backend of a pipeline if the APV and the PPV are unequal.

1 12. The method of claim 10, wherein determining the PPV by comparing includes  
2 comparing the lowest eighth or less of LSBs of the first operand to the lowest  
3 eighth or less of LSBs of the second operand.

1 13. The method of claim 10, wherein determining the PPV by comparing includes  
2 comparing for equality between the first and second pluralities.

1 14. A processor comprising:

2 a predicate history table;  
3 a register file;  
4 a predicted predicate value (PPV) calculator having a first input coupled to  
5 an output of the predicate history table and a second input coupled to  
6 an output of the register file; and  
7 a speculative predicate register file coupled to an output of the calculator.

1 15. The processor of claim 14, further comprising:

2 a IP select circuit having an output coupled to the predicate history table;  
3 a register select circuit having an output coupled to the register file; and  
4 an instruction decoder having an output coupled to input of the IP select  
5 circuit and the register select circuit.

1 16. The processor of claim 15, further comprising a pipeline having a PPV input  
2 coupled to an output of the file and an actual predicate value (APV) output  
3 coupled to an input of the predicate history table.

1 17. The processor of claim 16, further comprising an XOR gate having a first  
2 input coupled to the APV output of the pipeline, a second input coupled to an  
3 output of the file, and an output coupled to a flush input of the pipeline.

1 18. A processor comprising:

2 a predicate history table to store historical information associated with a  
3 predicate; and  
4 a predicted predicate value (PPV) calculator to calculate a PPV based on  
5 a comparison of a first plurality of least significant bits (LSBs) of a first  
6 operand to a second plurality of LSBs of a second operand.

1 19. The processor of claim 18, further comprising a speculative predicate register  
2 file to store the PPV.

1 20. The processor of claim 19, further comprising a pipeline to receive the PPV,  
2 and to conditionally execute a predicated instruction depending on the PPV.

1 21. The processor of claim 18, further comprising a pipeline to receive the PPV,  
2 and to conditionally execute a predicated instruction depending on the PPV.

1 22. The processor of claim 21, wherein the pipeline includes an actual predicate  
2 value output to provide an actual predicate value to the predicate history  
3 table.

1 23. The processor of claim 18, wherein the calculator includes a selector to  
2 select, based on a confidence level, the PPV to be based on either historical  
3 information or the comparison.

1 24. A system comprising:  
2 memory to store a first value;  
3 a bus to transfer the first value from the memory; and  
4 a processor to receive the first value from the bus and to compare a first  
5 plurality of least significant bits (LSBs) of the first value to a second  
6 plurality of least significant bits (LSBs) of a second value to calculate a  
7 predicted predicate value (PPV) for a predicate.

1 25. The system of claim 24, wherein the memory is main memory.

1 26. The system of claim 24, wherein the bus is a system bus.

1 27. The system of claim 24, wherein the processor further comprises a pipeline to  
2 receive the PPV, and to conditionally execute a predicated instruction  
3 depending on the PPV.

1 28. The system of claim 25, wherein the processor further comprises a predicate  
2 history table to store historical information associated with the predicate.